

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
				843454	114	2
NOTICE OF REFERENCES CITED				APPLICANT(S)	BLACHARD	

## U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
A	4 5 8 2 5 6 5	4-86	KAWAKATSU	29	580	8-8-84
B	4 5 0 9 2 4 9	4-85	GOTO ET AL.	29	576W	9-23-83
C	4 3 7 4 4 5 5	2-83	GOODMAN	29	580	
D	4 5 4 6 3 6 7	10-85	SCHUTTEN ET AL.	351	55	6-21-82
E	4 5 9 6 9 9 9	6-86	GOBRECHT ET AL.	351	55	3-22-84
F	4 3 4 5 2 6 5	8-82	BLACHARD	29	571	
G						
H						
I						
J						
K						

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG. PP. SPEC.
L	0 0 6 5 4 4 7	4-84	JAPAN	KAZUYA	29	576W	
M	0 1 0 8 3 2 5	6-84	JAPAN	TOSHIO	29	576W	
N							
O							
P							
Q							

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	UEDA, "A NEW VERTICAL POWER MOSFET STRUCTURE WITH EXTREMELY REDUCED ON-RESISTANCE," IEEE TRANS. ON ELECTRON DEVICES, VOL. ED-32, NO. 1 JUN. 85, PP. 2-6.
S	BALIGA, "THE INSULATED GATE TRANSISTOR; A NEW THREE-DIMENSIONAL TERMINAL MOS CONTROLLED DIPOLEAR POWER DEVICE," IEEE TRANS. ON ELECT. DEV. VOL. ED-31, JUN. 84, PP. 821-828
T	
U	

EXAMINER	DATE
T. Thomas.	12-17-86.

\*A copy of this reference is not being furnished with this office action.  
(See Manual of Patent Examining Procedure, section 707.05 (a).)